Claim Amendments

1-21. (Canceled).

22. (Previously presented) An apparatus for distributing reference voltages, comprising

a voltage reference circuit to develop the reference voltage,

a functional unit to operate based upon the reference voltage, and

a first switched capacitor transformer comprising a first capacitor and a first plurality of switches that couple the first capacitor to the voltage reference circuit in order to receive the reference voltage during a first period and that couple the first capacitor to the functional unit in order to deliver the reference voltage to the functional unit during a second period, and

a second switched capacitor transformer comprising a second capacitor and a second plurality of switches that couple the second capacitor to the voltage reference circuit in order to receive the reference voltage during the second period and that couple the second capacitor to the functional unit in order to deliver the reference voltage to the functional unit during the first period.

23. (Canceled).

24. (Previously presented) The apparatus as set forth in claim 22, further comprising:

a clock generator to switch first and second switches of the first switched capacitor transformer and third and fourth switches of the second switched capacitor transformer ON during the first period and to switch third and fourth switches of the first switched capacitor transformer and first and second switches of the second switched capacitor transformer ON during the second period, wherein the first and second periods are disjoint.

25. (Previously Presented) The apparatus as set forth in claim 24,

wherein the first and third switches are pMOSFETs, and the second and fourth switches are nMOSFETs.

26. (Previously presented) The apparatus as set forth in claim 22, wherein the first switched capacitor transformer further comprises

first and second input ports coupled to the voltage reference circuit;

first and second output ports coupled to the functional unit;

a second capacitor comprising a first terminal connected to the first input port and a second terminal connected to the second input port; and

a third capacitor comprising a first terminal connected to the first output port and a second terminal connected to the second output port.

27. (Previously presented) The apparatus of claim 22 further comprising a clock generator to control switching of the first plurality of switches and the second plurality of switches such that the first capacitor is not simultaneously coupled to both the voltage reference circuit and the functional unit and such that the second capacitor is not simultaneously coupled to both the voltage reference circuit and the functional unit.

28. (Previously presented) The apparatus as set forth in claim 22, further comprising a clock generator to

switch first and second switches of the first switched capacitor circuit ON and third and fourth switches of the first switched capacitor circuit OFF to couple the first capacitor to the voltage reference circuit and to decouple the first capacitor from the functional unit during the first period, and

switch first and second switches of the second switched capacitor circuit OFF and third and fourth switches of the second switched capacitor circuit ON to decouple the second capacitor from the voltage reference circuit and to couple the second capacitor to the functional unit during the first period.

29. (Previously presented) The apparatus as set forth in claim 22, further comprising a clock generator to

switch first and second switches of the first switched capacitor circuit OFF and third and fourth switches of the first switched capacitor circuit ON to decouple the first capacitor from the voltage reference circuit and to couple the first capacitor to the functional unit during the second period, and

switch first and second switches of the second switched capacitor circuit ON and third and fourth switches of the second switched capacitor circuit OFF to couple the second capacitor to the voltage reference circuit and to decouple the second capacitor from the functional unit during the second period.

30. (Previously presented) An integrated circuit comprising

a voltage reference circuit to provide a reference voltage,

a plurality of functional units that operate based upon the reference voltage, and

a plurality of switched capacitors, each switched capacitor to receive the reference voltage from the voltage reference circuit during a first time duration of a clock and to deliver the reference voltage to at least one functional unit of the plurality of functional units during a second time duration of the clock.

31. (Previously presented) The integrated circuit of claim 30 wherein a functional unit of the plurality of functional units comprises an amplifier and the reference voltage biases the amplifier.

32. (Previously presented) The integrated circuit of claim 30 wherein a functional unit of the plurality of functional units comprises a phase lock loop having a frequency defined by the reference voltage.

33. (Previously presented) The integrated circuit of claim 30 wherein a functional unit of the plurality of functional units comprises a voltage regulator having an output voltage defined by the reference voltage.

34. (Previously presented) The integrated circuit of claim 30 wherein each of the plurality of switched capacitors comprises a capacitor and a plurality of switches to couple the capacitor to the reference voltage during the first time duration and to decouple the capacitor from the plurality of functional units during the first time duration.

35. (Previously presented) The integrated circuit of claim 34 wherein each of the plurality of switched capacitors comprises a capacitor and a plurality of switches to decouple the capacitor from the reference voltage during the second time duration and to couple the capacitor to at least one functional unit of the plurality of functional units during the second time duration.

36. (Previously presented) The integrated circuit of claim 35 wherein the first time duration and the second time duration are non-overlapping.

37. (Previously presented) A method comprising

generating a reference voltage,

coupling the reference voltage to a first capacitor and decoupling a functional unit from the first capacitor to develop the reference voltage across the first capacitor during a first period of a clock, and

decoupling the reference voltage from a second capacitor and coupling a functional unit to the second capacitor to provide the functional unit with the reference voltage during the first period of the clock.

38. (Previously presented) The method of claim 37 further comprising

decoupling the reference voltage from the first capacitor and coupling the functional unit to the first capacitor to provide the functional unit with the reference voltage during a second period of the clock, and

coupling the reference voltage to the second capacitor and decoupling the functional unit from the second capacitor to develop the reference voltage across the second capacitor during the second period of the clock.

39. (Previously presented) The method of claim 37, further comprising setting a frequency of the functional unit based upon the reference voltage.

40. (Previously presented) The method of claim 37, further comprising setting an output voltage of the functional unit based upon the reference voltage.

41. (Previously presented) The method of claim 37, further comprising biasing the functional unit based upon the reference voltage.

42. (Previously presented) The method of claim 37, wherein the first period and second period are non-overlapping.